IC/semiconductors(LOGIC, MEMORY, Analog + OSD)

(OSD: Optoelectronic, Sensor, and Discrete components)

3Dx3D x3D

Chee Wee Liu (劉致為)

Distinguished/Chair Professor / IEEE Fellow,

National Taiwan University

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http://nanosioe.ee.ntu.edu.tw

High mobility/high K/FinFET

PPACR (performance, power, area, cost, reliability)

Google Scholar Page

(Citation :8421/ H index:41 / i10 index:205

https://www.digitimes.com.tw/seminar/DWebinar_20220824/

Distinguished/Chair (特聘/講座) Professor/IEEE Fellow
Department of Electrical Engineering (電機工程學系),
Graduate Institute of Electronics Engineering (電子工程學研究所),
Graduate Institute of Photonics and Optoelectronics engineering (光電工程學研究所),
Center of Condensed Matter Sciences (凝態科學研究中心)
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Google Scholar Page (Citation: 8395 / H index: 41 / i10 index: 202)
Research.com (D-index 33, Citation 5821)
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NARlabs
Industry Academia Innovation School (產學創新研究學院),
National Yang Ming Chiao Tung University
College of Semiconductor Research (半導體研究學院),
National Tsing Hua University
Graduate School of Advanced Technology (重點科技研究學院),
National Taiwan University

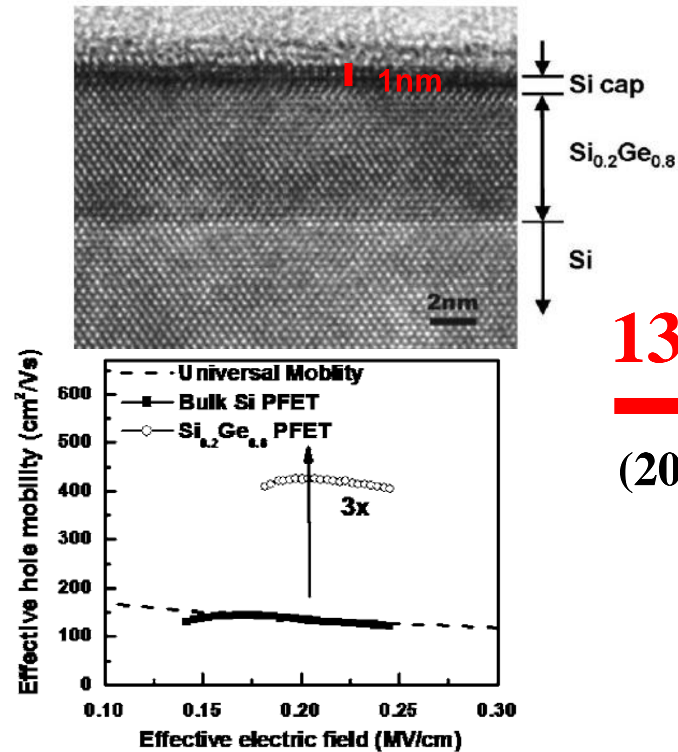
1. 2023 FutureTeck Award (未來科技獎)
2. 2023 VLSI-TSA (International Symposium on VLSI Technology, Systems and Application) Best Poster Paper Award (advisor)
3. 2023 VLSI-TSA (International Symposium on VLSI Technology, Systems and Application) Best Student Paper Award (advisor)
4. 2022 MRS-T華立創新材料大賽 金質獎 (Wah Lee Material Innovation Golden Award)
5. 2022 TECO Award 東元獎 (電資/資訊/通訊科技)
6. 2022 FutureTeck Award (未來科技獎): High mobility channel/process/stacked channel/thermal modeling (高遷移率材料、製程、多層疊元件及熱電路模型)
7. 2022 FutureTeck Award (未來科技獎): Advanced stacked Chips (前瞻單晶片三維多層級堆疊之高密度積體電路關鍵技術)
8. 2022 VLSI-TSA (*International Symposium on VLSI Technology, Systems and Application*) Best Student Paper Award (advisor)
9. 2021 International Electron Device Meeting (IEDM) Roger A. Haken Best Student Paper Award (advisor) IEDM Roger A. Haken Best Student Paper Award — IEDM (ieee-iedm.org)
10. 2021 Pan Wen Yuan Foundation Outstanding Research Award (潘文淵文教基金會研究傑出獎)
11. 2021 Best Paper Advisor Award, 1th SNDCT (*Symposium on Nano-Device Circuits and Technologies*) 傑出論文指導教授獎
12. 2002 Semiconductor Research Corporation Cross-discipline Semiconductor Research Award (CMOS photonics)

- **SiGe/GeSn epi/photonics, stacked 3D transistors, RF device and circuit/thermal simulation (physics-based and machine learning-based), IGZO TFT, SRAM/MIM/FTJ, FRAM, FeFET/MTJ/SOT/DRAM, and CMOS image sensors.**
- **The tallest transistor (8/16/24 stacked channels), the record high 2,400,000 cm^2/Vs electron mobility in strained Si, the first Si-capped SiGe/Ge channels with 3x mobility enhancement (in 5nm node production now), the first CVD GeSn outperforming MBE in terms of hole mobility, the first stacked GeSn/GeSi channel GAA(nanosheet/nanowire) transistors, the first Si/SiGe/SiC MIS LED/photodetectors, and invented tree/E transistors, CFET beyond Stacked GAA.**
- 700+ papers (269+ journal papers, 33 IEDM, 18VLSI), 76 US patents, 2 China patents, 50 Taiwan ROC patents, more than 8391+ citations with h-index=41
- **44 Ph.D. graduates, and 143 master graduates. 6 graduate students as professors (2NTU, 1 NTNU, 1 NCHU, 1 NDHU, 1 NJUST), and 3 postdocs as professors (1 NTU, 1 NCU, 1 CGU). Currently, he is advising 26 PhD students and 21 masters.**

VP/Senior Director /Director/Dept. Manager / Manager /Engineer in tsmc/NTC/Innolux/MXIC/ASML/Samsung/Intel/….

MOST advanced FinFET on the market

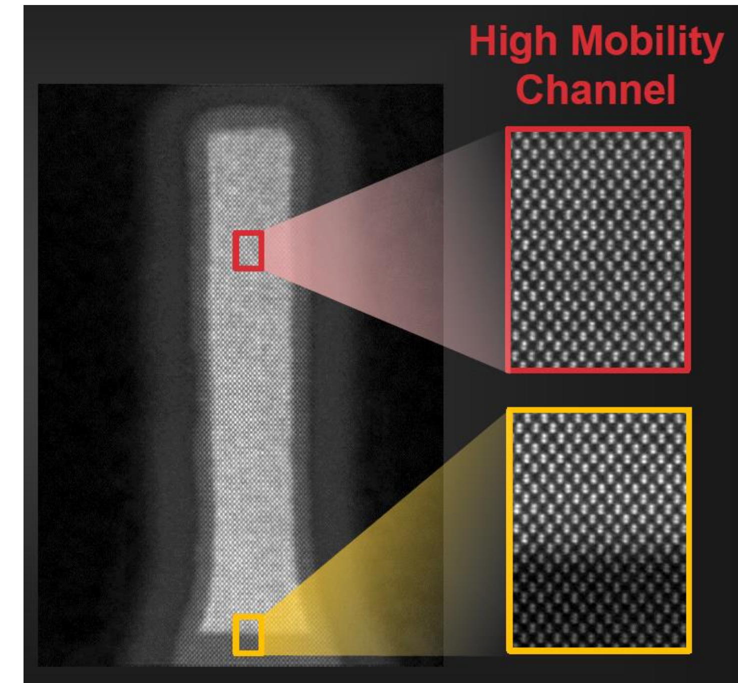
2007 APL



13 years

(2007-2020)

2021 TSMC ISSCC

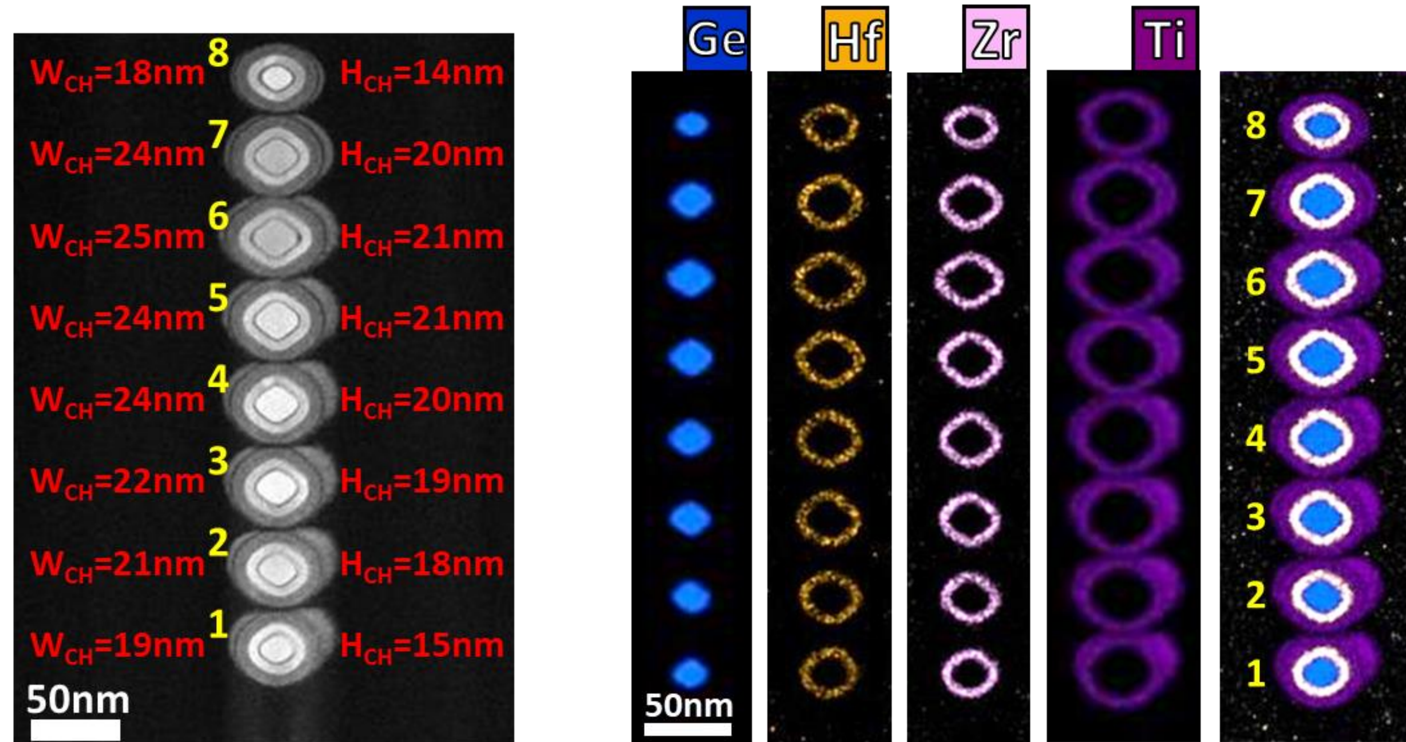


Mark Liu, Plenary Session 1.1, ISSCC 2021.

C.-Y. Peng, F. Yuan, C.-Y. Yu, P.-S. Kuo, M. H. Lee, S. Maikap, C.-H. Hsu, and C. W. Liu, Appl. Phys. Lett. 90, 012114 (2007) .(Cited No./Self Cited No.= 30/ 7)

- $Si_{0.2}Ge_{0.8}$ channel with 1nm Si cap, having higher mobility(3X) than Si.
- It takes 13 years to commercialize HMC.

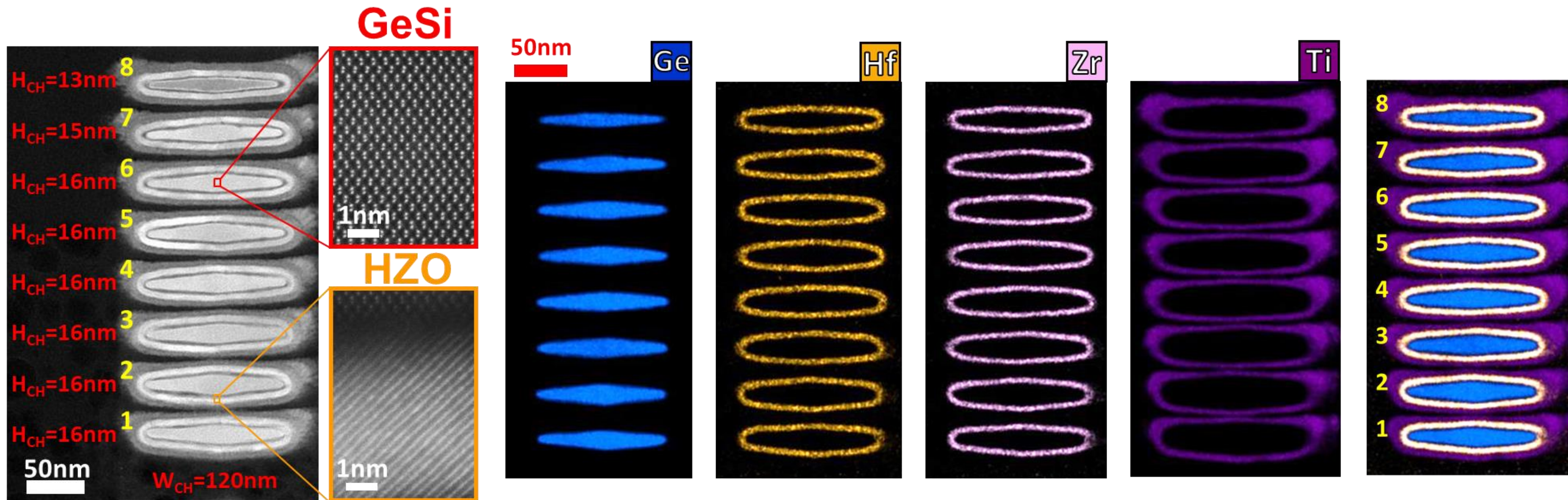
8 $Ge_{0.95}Si_{0.05}$ Nanowires with High-κ $Hf_{0.2}Zr_{0.8}O_2$ (2023 VLSI)



Yi-Chun Liu, Yu-Rui Chen *et al.*, *VLSI*, T16-4, 2023.

- **The 8 nanowires are surrounded by $Hf_{0.2}Zr_{0.8}O_2$ and *in-situ* TiN to ensure the GAA structure.**

8 $Ge_{0.95}Si_{0.05}$ Nanosheets with High-κ $Hf_{0.2}Zr_{0.8}O_2$ (2023 VLSI)

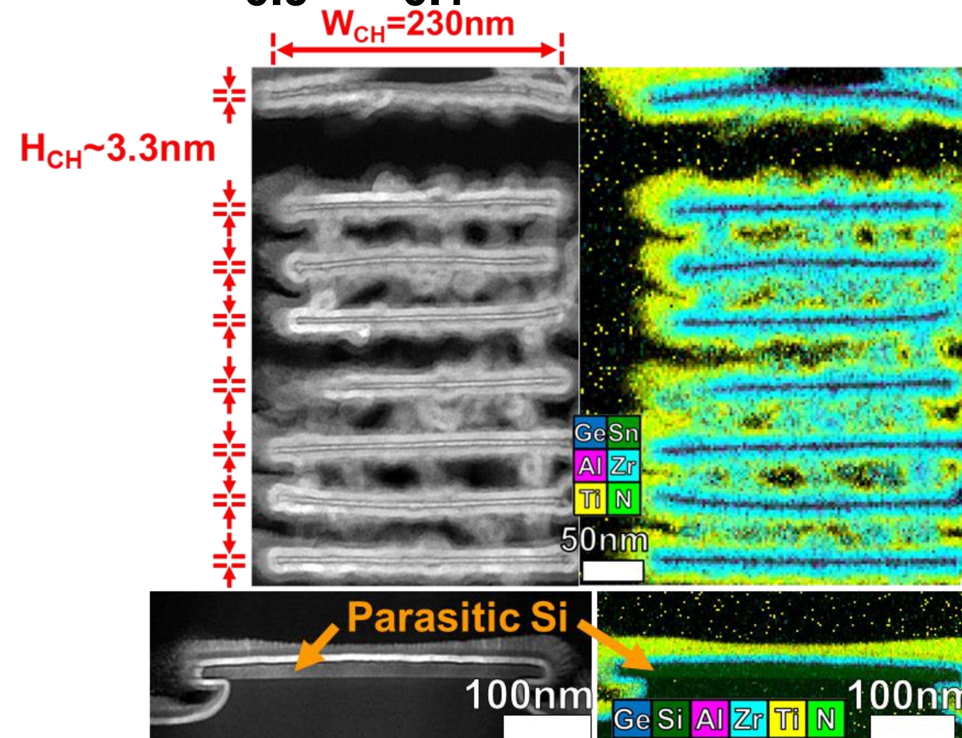


Yi-Chun Liu, Yu-Rui Chen *et al.*, *VLSI*, T16-4, 2023.

- The 8 nanosheets are surrounded by $Hf_{0.2}Zr_{0.8}O_2$ and *in-situ* TiN to ensure the GAA structure.

IEDM Roger A. Haken Best Student Paper Award — IEDM (ieee-iedm.org)

8 Stacked Wide $Ge_{0.9}Sn_{0.1}$ Ultrathin Bodies (2021 IEDM)

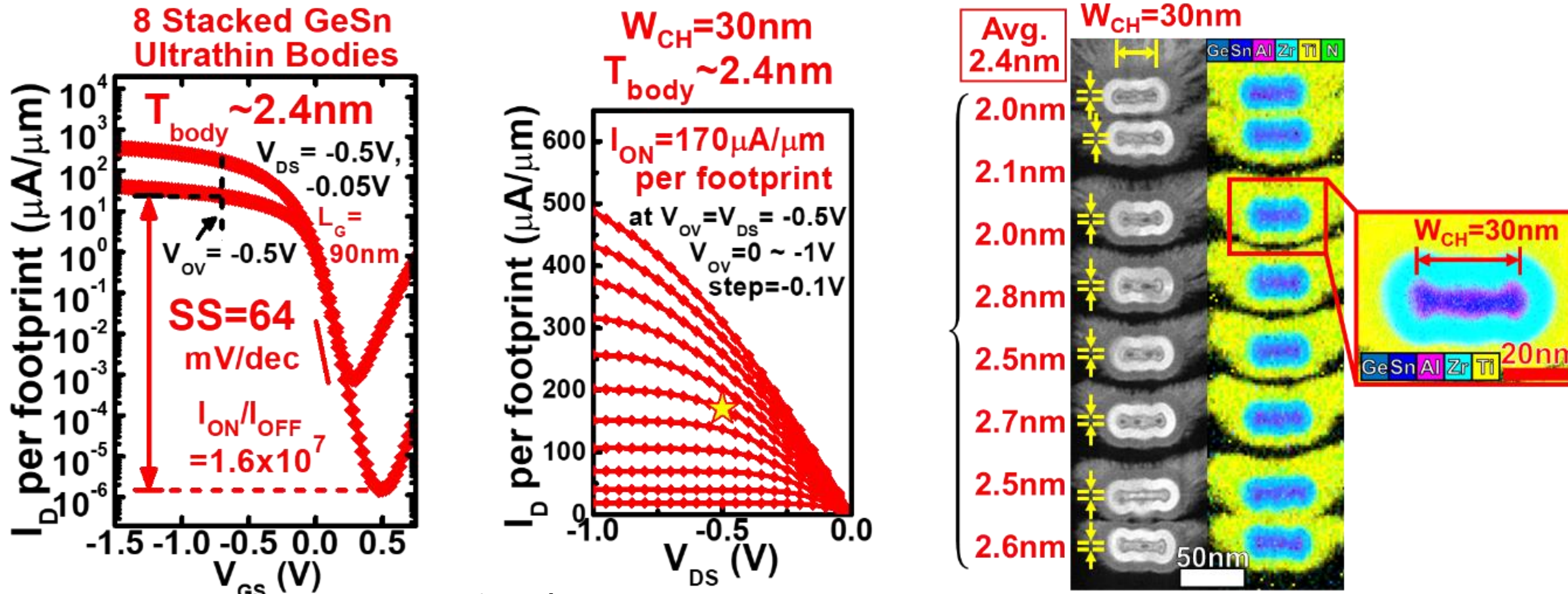


C.-E. Tsai *et al.*, *IEDM*, 2021, pp. 569.

- The ~3.3nm GeSn ultrathin bodies with good vertical uniformity and very high aspect ratio of 70.

(W_{CH}/H_{CH}=230/3.3)

$Ge_{0.9}Sn_{0.1}$ Ultrathin Bodies (2022 VLSI)



C.-E. Tsai *et al.*, *VLSI*, 2022, pp. 401.

- T_{body}~2.4nm with record low SS=64mV/dec and high $I_{ON}/I_{OFF}=1.6\times10^7$ at V_{DS}= -0.05V among GeSn pGAAFETs.
- I_{ON}=170μA/μm per footprint normalized by W_{CH}=30nm.

Saturday 2:20-4pm graphic MOS lecture

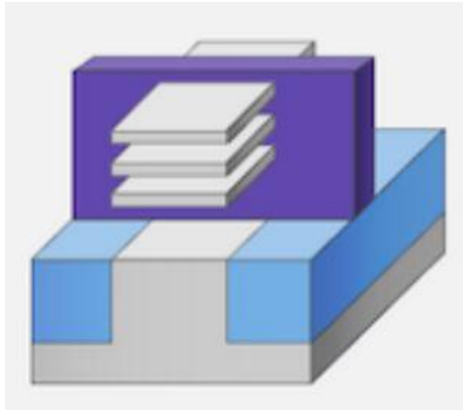
- Free handout
- Free textbook
- Free schedule
- Cyclic
- Welcome to join 2-4 pm on Sat

(DIGITIMES ASIA) Taiwan's award-winning student paper shows breakthrough in stacking GeSn nanosheet transistors

華立創新材料大賽 產學無縫接軌

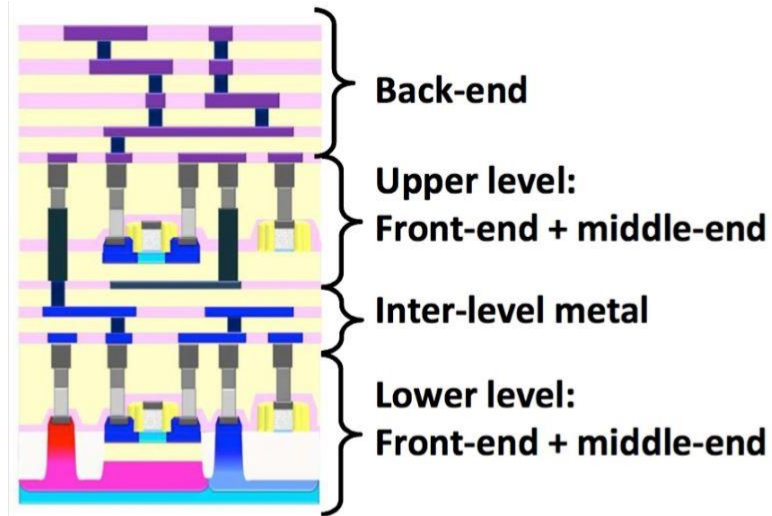
3Dx3Dx3D

3D



Channel stacking

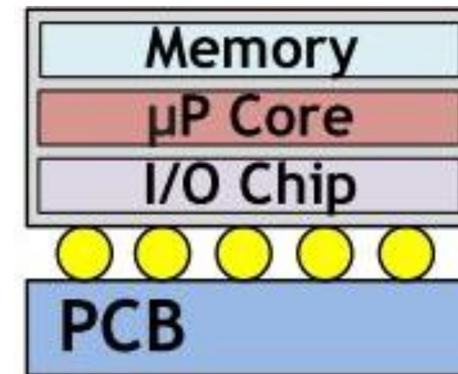
3D



Transistor stacking

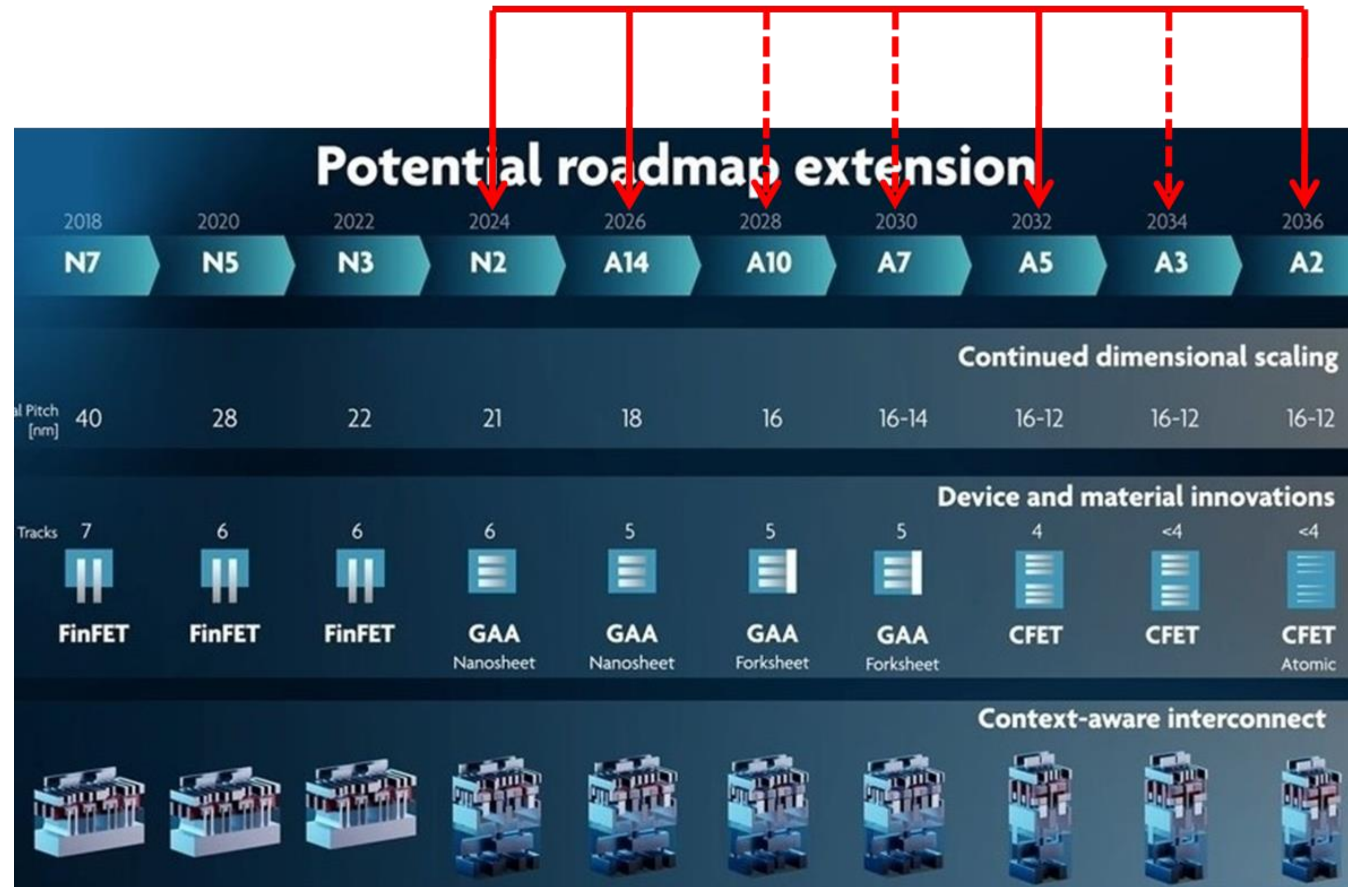
Monolithic /Sequential (w/ BEOL)

3D (Far backend/ Heterogeneous integration)



- Dielets/Chiplet Stacking
- SOIC (tsmc)
- X-Cube (Samsung)
- FOVEROS (Unique and special in Greek) /EMIB (Intel)

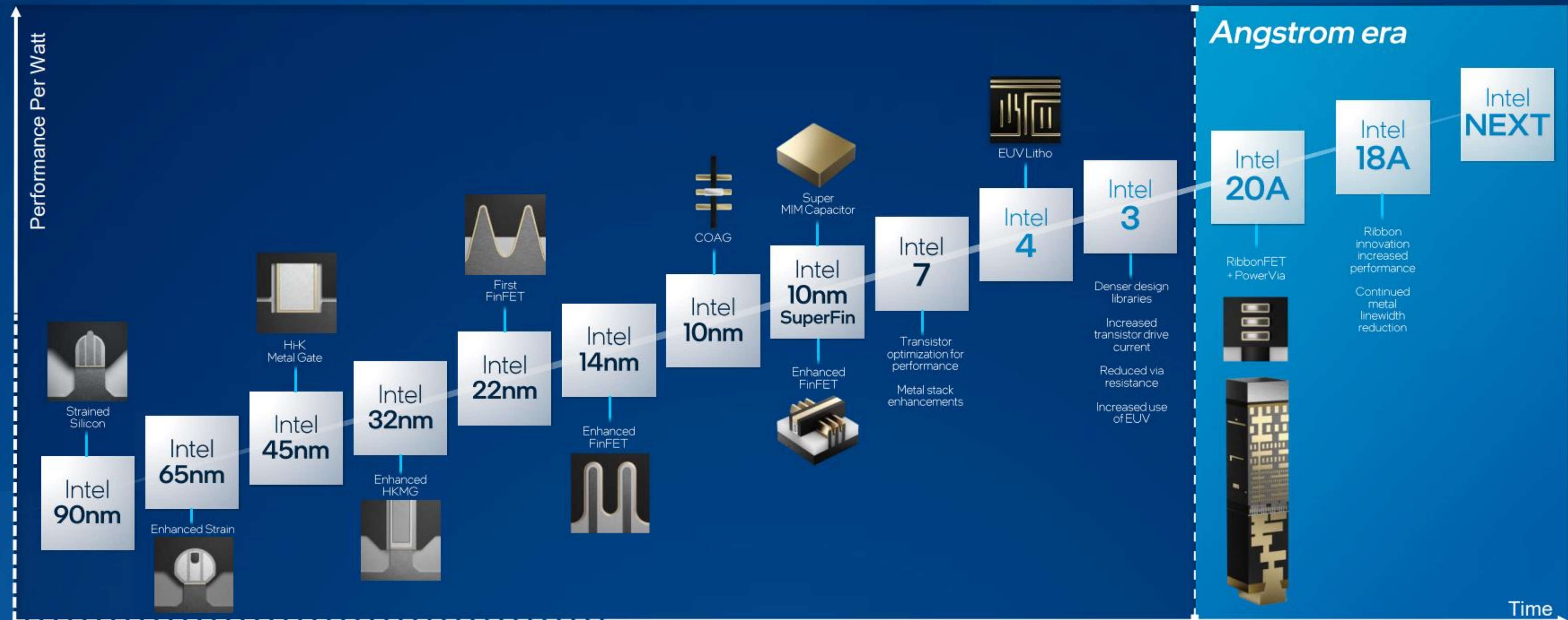
Device roadmap for More Moore scaling



Solid line: Proceeding work
Dash line: Future work

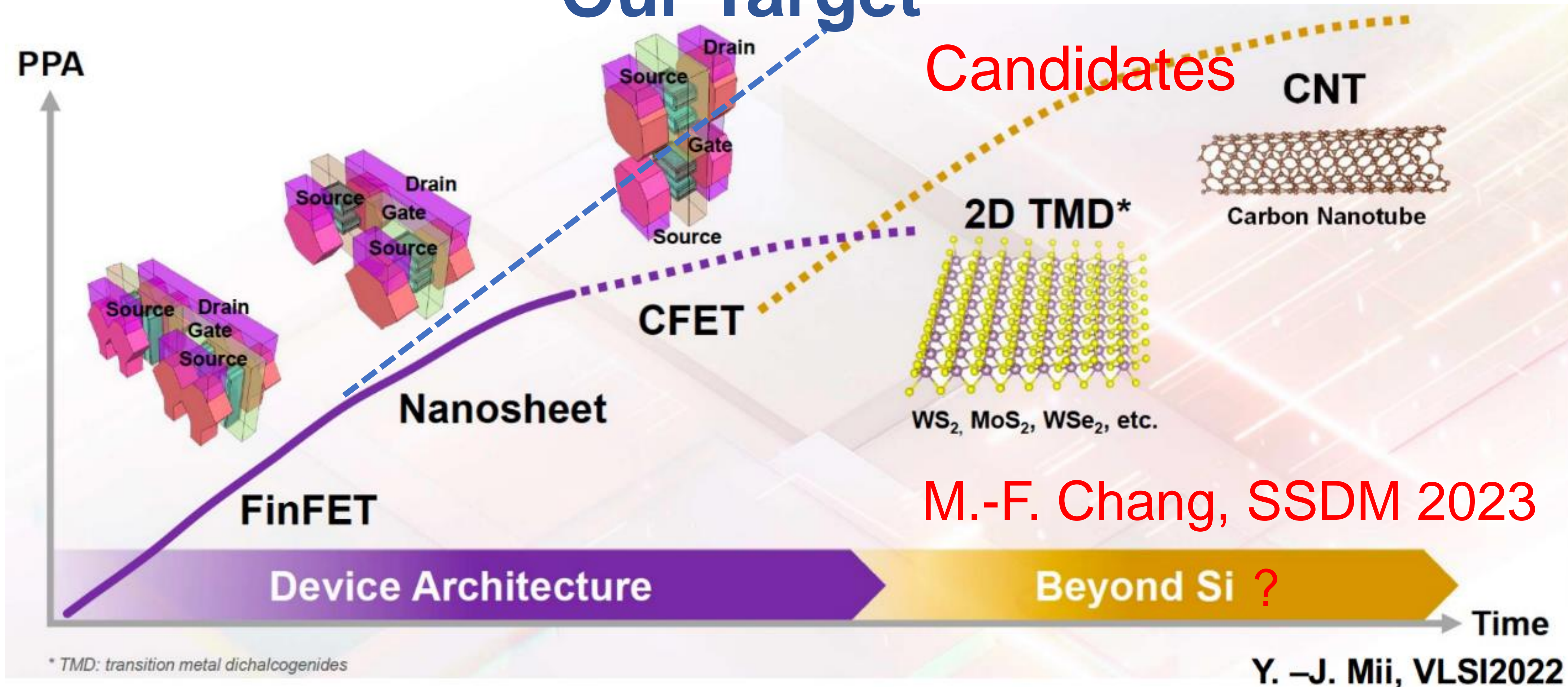
Source IMEC 2022 potential roadmap.

- **CFET (transistor stacking, nFET on pFET or p on n) starts at A5 (0.5nm node)**
- **Atomic (2D) in A2 node (0.2 nm node)**
- **We have demonstrated highly stacked nanosheets/nanowires, TreeFET, CFET, and ultrathin bodies.**



- **Intel 20A & 18A(Angstrom Era) → 1st RibbonFET(4 stacked channels) + Power Via**
- **TSMC GAA 2nm/Samsung GAA 3nm**

Device Architecture Outlook



- CFET after nanosheets, 2D after CFETs
- Innovations are needed to improve CFET/nanosheet slope.

Research topics

- **CMOS(channel stacking, 1nm and beyond)**
  Stacked Nanosheet **/King/tree channel Thermal modeling**
  Photoluminescence and photo response
- **Transistor Stacking (A5 and beyond)**

CFET n/p or p/n

SRAM

IGZO (backend transistor) 3D integration

- FeFET/MIM/FTJ/DRAM
- CMOS image sensor
- 3 tier Epitaxial 3D IC for Beyond A2

2023 VLSI 論文統計 (technology + Joint Focus Session)

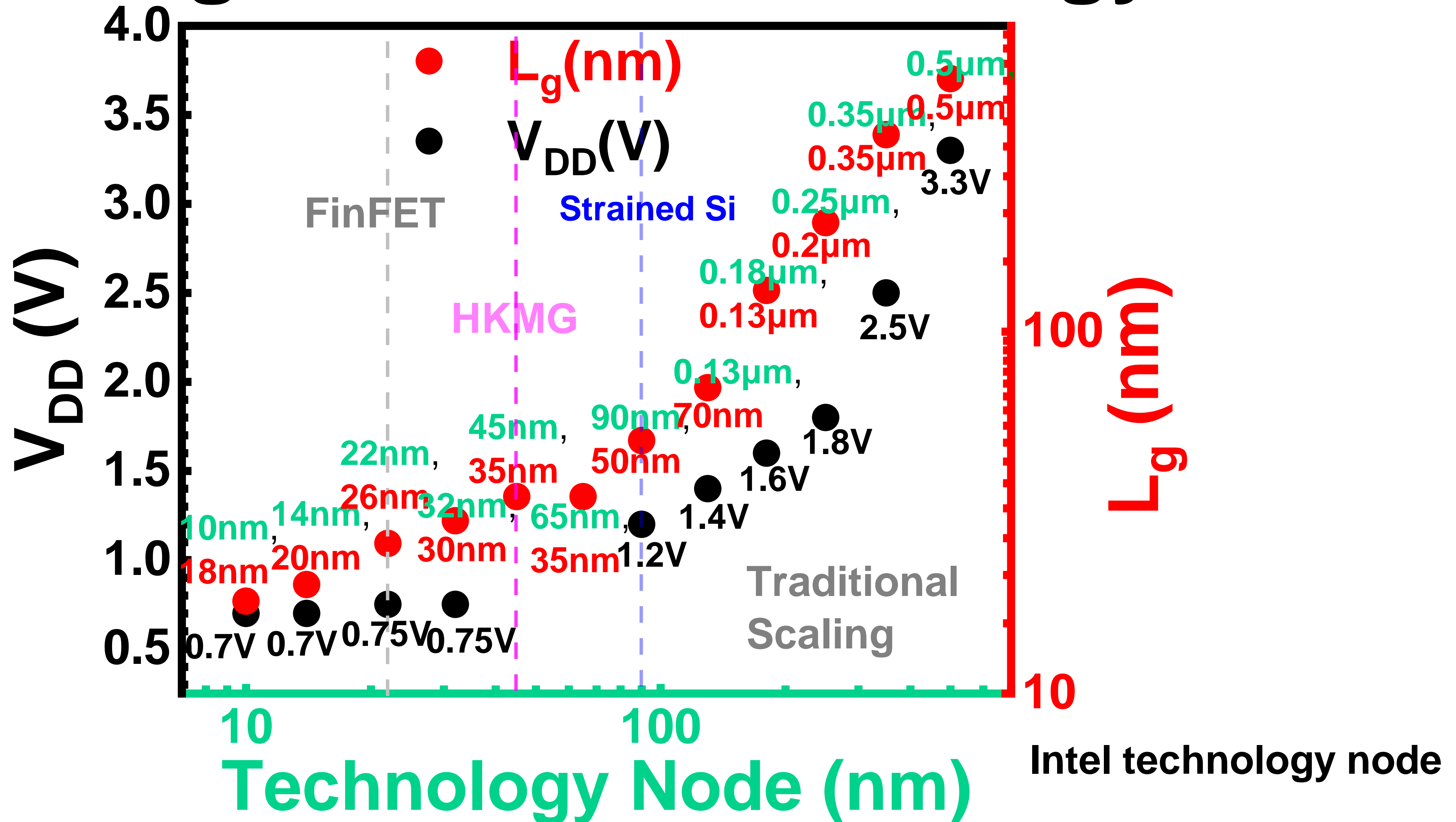
Affiliation	Session	Total number
TSMC	T1-4, T8-1, T13-3, T15-3, T16-1, JFS4-2(invited)	6
National Taiwan Univ (劉致為)	T5-3, T12-4, T16-4, T17-3, T10-2(第一作者affiliation同時屬台大與師大，為劉致為教授學生, 與李敏鴻教授合作),	5
National Yang Ming Chiao Tung Univ	T14-2, T18-5, T2-4 (第一作者affiliation同時屬陽交大與師大)	3
National Taiwan Normal Univ	T2-4, T10-2	2
National Tsing Hua Univ	T9-4	1
Industrial Technology Research Institute of Taiwan, Taiwan	T18-5	1

- The survey is based on the affiliation of the first author.

2023 IEDM Session: 3D Stacked Transistors

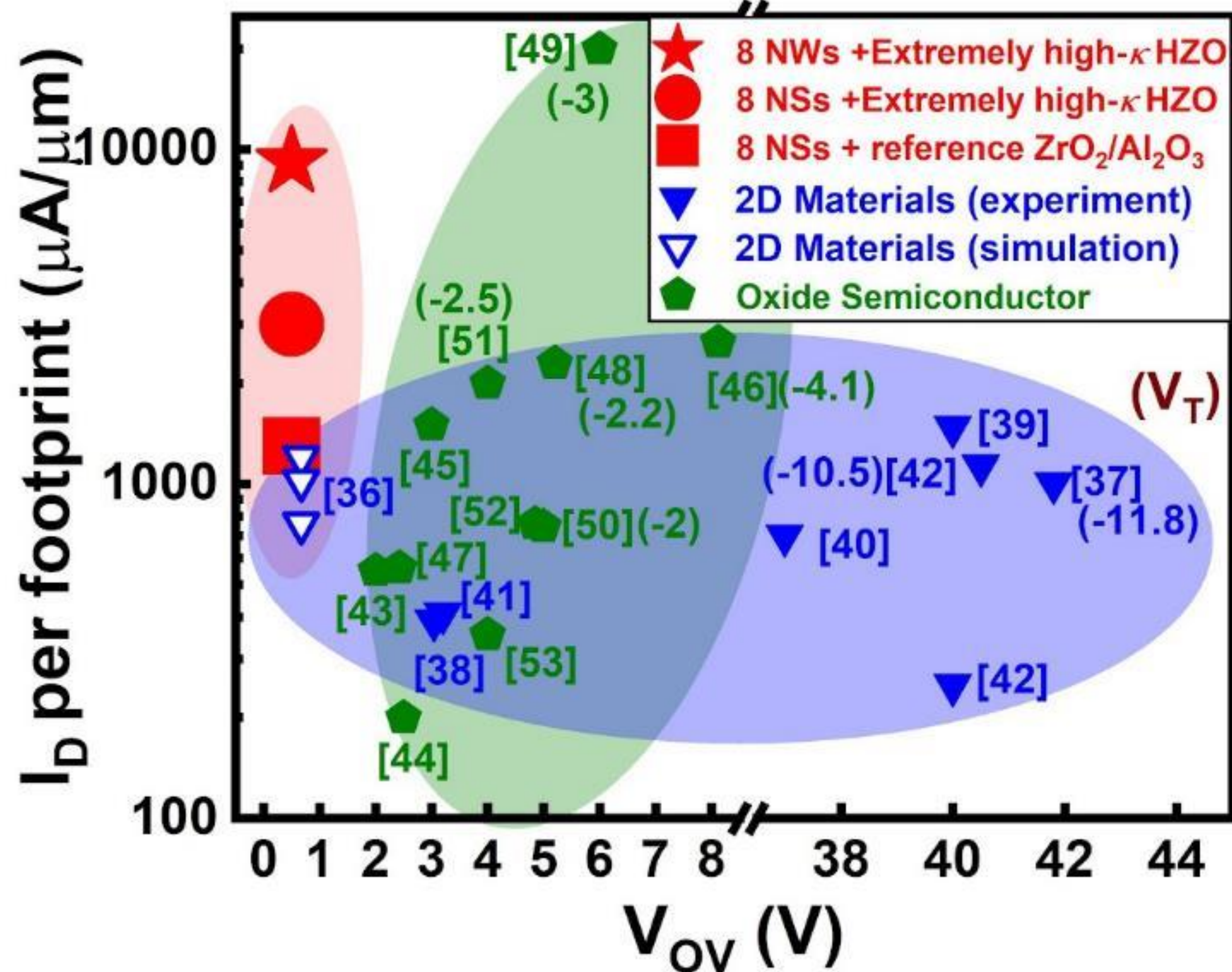
1. 3D Stacked Devices and MOL Innovations for Post-Nanosheet CMOS Scaling – **imec**
2. Demonstration of a Stacked CMOS Inverter at 60nm Gate Pitch with Power Via and Direct Backside Device Contacts – **Intel**
3. 3D Sequential Integration with Si CMOS Stacked on 28nm Industrial FDSOI with Cu-ULK iBEOL Featuring RO and HDR Pixel – **CEA-Leti**
4. First Demonstration of 3-dimensional Stacked FET with Top/bottom Source-drain Isolation and Stacked n/p Metal Gate – **Samsung Electronics**
5. First Demonstration of Monolithic Self-aligned Heterogeneous Nanosheet Channel Complementary FETs with Matched V_T by Band Alignments of Individual Channels – **NTU**
6. Complementary Field-Effect Transistor (CFET) Demonstration at 48nm Gate Pitch for Future Logic Technology Scaling – **tsmc**

V_{DD} Scaling Trend vs Technology Node



- For V_{DD} scaling, the V_{DD} of advanced CMOS becomes lower than 0.7V.

Benchmark of nFETs (Si-based/2D/OS)

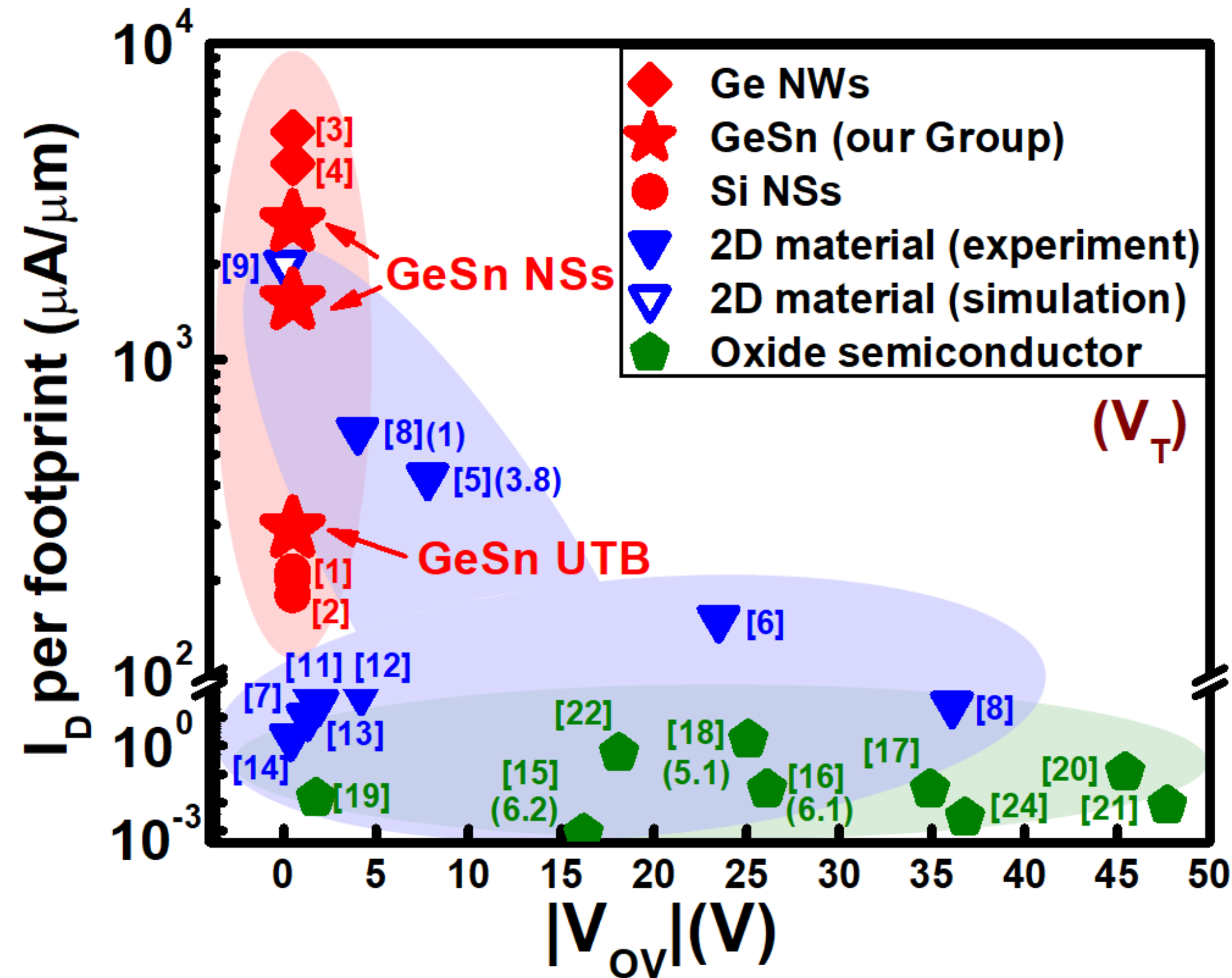


2D		
[36]	2D simulation	M. Luisier et al., IEDM, 2016
[37]	Bi-1L MoS_2 (BG)	Shen, PC. et al., Nature 593, 211–217, 2021.
[38]	MoS_2 back gate (BG)	A.-S. Chou et al., VLSI, 2020.
[39]	MoS2 Back Gate	C. J. Mcclellan et al., ACS Nano, 2021, Stanford
[40]	GAA MoS2	Y. Y. Chung et al. IEDM 2022, TSMC
[41]	Bi-1L MoS_2 (BG)	P.C. Chen et al., Nature, 2021, MIT
[42]	MoS_2	S. Ghosh et al., VLSI, 2023
OS		
[43]	IWO double gate (DG)	H. Ye et al., IEDM, 2020, 28.3.
[44]	IWO BG	W. Chakraborty et al., VLSI, 2020.
[45]	DG IGZO	W. Lu et al IEDM 2022, CAS
[46]	BG In2O3	Liao et al VLSI 2022, Purdue
[47]	BG ZnO	Chand et al VLSI 2022, NUS
[48]	DG ITO	Wahid et al IEDM 2022, Stanford
[49]	GAA In2O3	Z. Zheng et al IEDM 2022, Purdue, 4-3
[50]	In2O3	D. Zheng et al., VLSI, 2023
[51]	ITO	Y. Kang et al., VLSI, 2023,
[52]	ITO-IGZO	S. Hooda et al., VLSI , 2023
[53]	IGZO	J. Zhang et al., VLSI, 2023

•Accepted by TED 2023, Sept.

- **Negative V_t and large V_{OV} are not acceptable for advanced IC.**

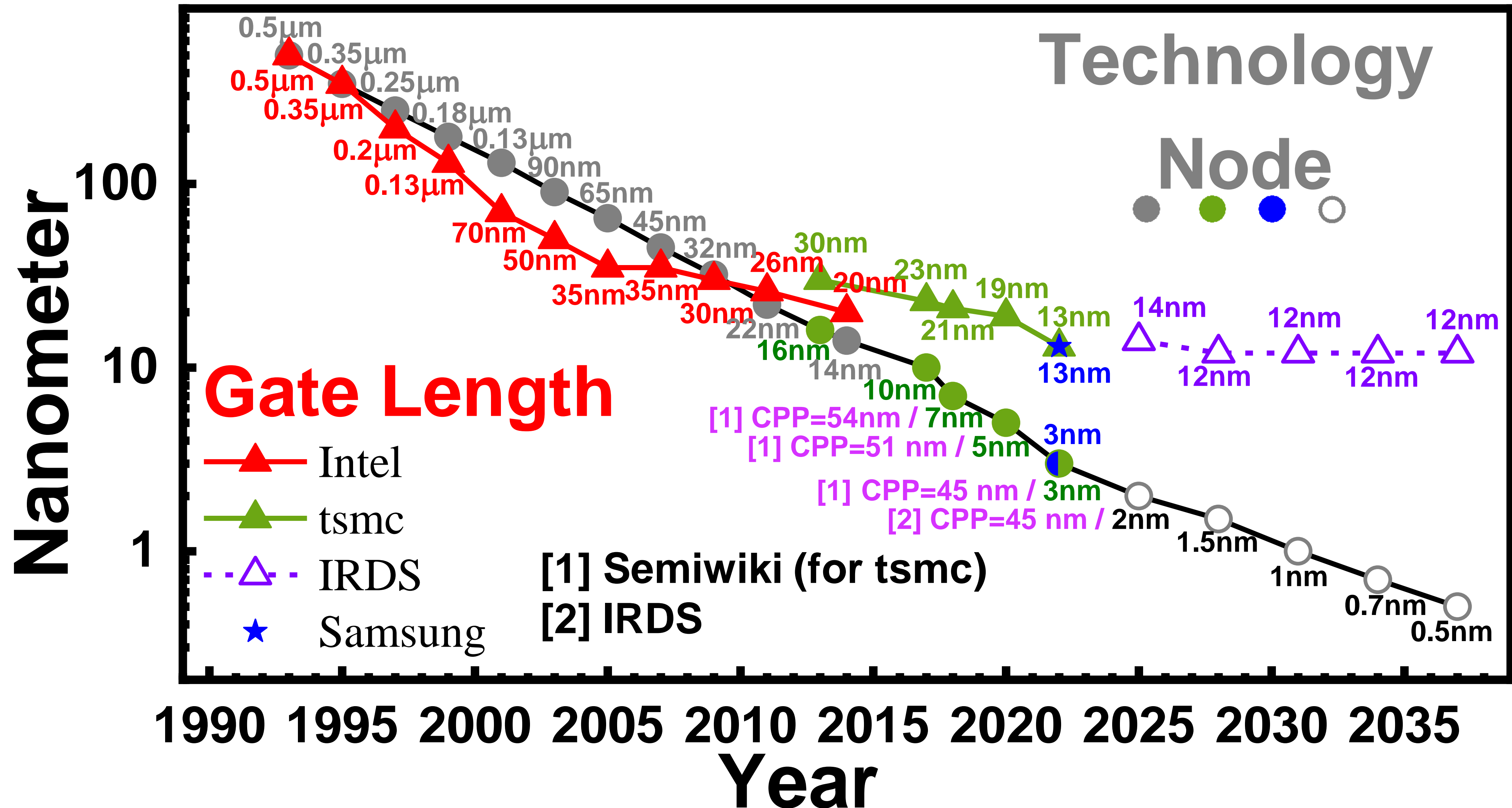
Benchmark of pFETs (Si-based/2D/OS)



Si-based		
[1]	Si NS	N. Shanker, et al., IEDM, 2022, 34.3.
[2]	Si NS	H. Mertens, et al., VLSI, 2023, T1-3.
[3]	Ge NW	E. Capogreco et al., VLSI, 2019, pp. T94.
[4]	Ge NW	H. Arimura et al., IEDM, 2020, pp. 11.
2D		
[5]	WSe_2 (BG)	Xinhang Shi, et al., IEDM, 2022, 7.1.
[6]	WSe_2 (BG)	Ang-Sheng Chou, et al., IEDM, 2022, 7.2.
[7]	WSe_2 (TG)	Terry Y.T. Hung, et al., IEDM, 2022, 7.3.
[8]	WSe_2 (TG)	Xiong Xiong, et al., IEDM, 2022, 20.6.
[9]	WSe_2 (DG)	Ning Yang, et al., IEDM, 2022, 28.1.
[10]	WSe_2	C. H. Naylor, et al., VLSI, 2023, T14-3.
[11]	WSe_2 (BG)	K. Maxey, et al., VLSI, 2022, TFS1-3.
[12]	WSe_2 (BG)	K. P. O'Brien, et al., IEDM, 2021, 7.1.
[13]	WSe_2 (GAA)	Xiong Xiong, et al., IEDM, 2021, 7.5.
[14]	WS_2 (TG)	Chao-Ching Cheng, et al., VLSI, 2019, T19-2.
OS		
[15]	SnO (BG)	Yun-Shiuan Li, et al., EDL, 2016.
[16]	SnO (BG)	Min-Gyu Shin, et al., Materials 2020, 13(14), 3055.
[17]	SnO (BG)	Myeong Gil Chae, et al., ACS Appl. Electron. Mater. 2023, 5, 1992−1999
[18]	SnO (BG)	Hye-Mi Kim, et al., ACS Appl. Mater. Interfaces 2021, 13, 30818−30825
[19]	SnO (BG)	P.-C. Chen, et al., Journal of Display Technology, vol. 12, no. 3, pp. 224-227, March 2016.
[20]	Ga:Cu_2O (BG)	Jun Hyeon Bae, et al., ACS Appl. Mater. Interfaces 2020, 12, 38350−38356.
[21]	CuO (BG)	Yu Yang, et al., Applied Surface Science 481 (2019) 632–636.
[22]	CuO_x (BG)	Wanjoo Maeng, et al., Ceramics International, 42 (2016), 5517–5522.
[23]	Cu_2O (BG)	Sang Yun Kim, et al., ACS Appl. Mater. Interfaces 2013, 5, 2417−2421.

- Performances of 2D and OS are quite behind Si-based.
- IC design needs PFETs and NFETs

L_G Scaling with Different Technology Node



- L_G can be larger than node name due to narrow width in footprint.

2D Materials for 1 nm (吳志毅教授)

自由財經

台大攜手台積電、MIT 為半導體產業開創新路

研究團隊由左至右為沈品均博士、吳志毅教授、周昂昇博士。（台大提供）.
〔記者林曉雲／台北報導〕台大攜手台積電、美國麻省理工學院（MIT）研究...

2021年5月14日

中央社

台大跨國二維材料研究 有助半導體產業邁向1奈米

台大今天發出新聞稿，由電機系暨光電所教授吳志毅等人，與台灣積體 ... 隨後
由台積電技術研究部門將鉍沉積製程優化，台大團隊則運用氦離子束微影...

2021年5月14日

數位時代

離1奈米更近了！台積電攜手台大提出半導體新材料「鉍」，有 ...

台灣大學、台積電與麻省理工學院（MIT）共同發表研究，首度提出利用「半 ...
台大電機系暨光電所吳志毅教授進一步說明，使用鉍為接觸電極的關鍵結構...

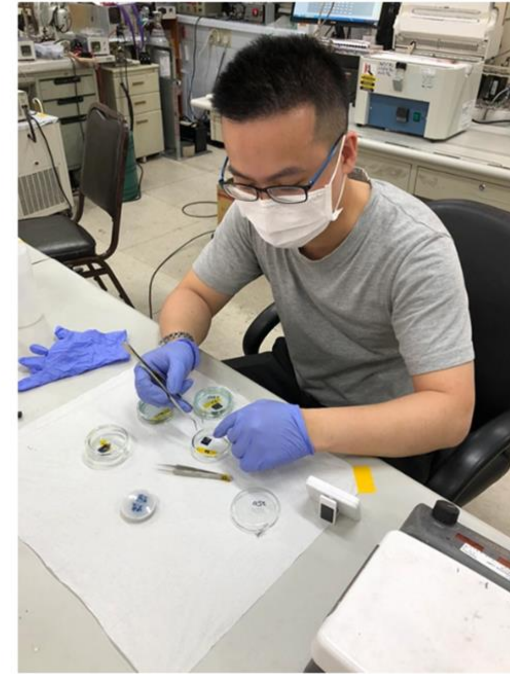
2021年5月14日

TSMC approaching 1 nm with 2D materials breakthrough

edn.com/tsmc-approaching-1-nm-with-2d-materials-breakthrough/

November 3, 2022
By Majeed Ahmad

TSMC's 1-nm chip manufacturing process is starting to take shape. After the findings of its collaboration with MIT and the National University of Taiwan (NTU) were made public this summer, TSMC is reportedly planning a 1-nm fab in Taoyuan, Taiwan. According to a report published in *Taiwan News*, the new 1-nm chip production facility will be located in an industrial park in Longtan District, where TSMC is already running two semiconductor packaging and testing plants.



Combining semimetallic bismuth electrodes with 2D materials can significantly reduce resistance and increase current conduction. Source: National University of Taiwan

成果目標 ： ■前端元件　□ 後段連接　□新穎材料

台積電-臺灣大學聯合研發中心
TSMC - NTU JOINT RESEARCH CENTER
tsmc
Planar FET
GAAFET
FINFET
GAAFET